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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WERNER, BRIAN P	

ART UNIT	PAPER NUMBER
2621	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/848,479	GUEST ET AL.	
	Examiner	Art Unit	
	Brian P. Werner	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 29 October 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 73-98 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 73-98 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's claim amendments and arguments filed on October 29, 2004 have been entered. Claims 73-98 remain pending.

Response to Arguments

2. Each of the remarks and/or arguments filed on October 29, 2004 have been considered:

Claim Objections:

In response to the amendment to claim 98, the previous claim objection under Rule 75 is withdrawn.

Double Patenting:

In response to the Terminal Disclaimer filed on August 3, 2004, the previous Double Patenting rejection is withdrawn.

Prior Art Rejections:

The applicant's arguments and remarks regarding the Sumie reference are moot in view of the new grounds of rejection advanced below.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 73-75, 79-81, 90-92 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Sumie et al. (US 5,943,437 A) and Gallarda et al. (US 6,539,106 B1).

The Sumie Reference

Sumie discloses a system for detecting defects on semiconductor dies (figure 6; "detect the defect" and "(die) repeated appears" at column 8, lines 49-51); comprising:

a die image comparator (figure 6, numeral 3a) creating a difference image by subtracting ("difference is calculated pixel by pixel" at column 5, line 31; figure 7, numeral S2) a reference die image ("reference image" at column 5, line 29) and an inspection die image ("inspection image" at column 5, line 28); and

a difference image analysis system for detecting defects from the difference image as well as their "position" and "type" (column 8, lines 61-68).

Sumie teaches storing the reference die image in a memory (the reference image is stored in memory 3c of figure 6).

Regarding claim 74, Sumie disclose an imaging system creating a digital image (figure 6, numeral 2).

Regarding claim 75, the Sumie stores the die images at figure 6, numerals 3b and 3c.

Difference

While Sumie teaches the concept of a defect free "reference image" for subsequent comparison with an inspection image,

where "the reference image data Idc to be stored in the image memory 3c of the image processor 3 ... may be data of an image obtained by picking up an image of a portion of the surface of the semiconductor wafer where there is no defect" at column 7, line 55,

and while Sumie states that an "image of the semiconductor wafer 1 in a position where no defect exists is further picked up to use as a reference image" at column 9, line 1,

Sumie does not describe how the "image of a portion of the surface of the semiconductor wafer where there is no defect" (column 7, line 55) is determined in the first place. Thus, Sumie does not explicitly teach determining whether a first or second image can be used as the reference image by creating a difference image without a manually selected reference.

Note: Applicant argues in the response received on October 29, 2004 that Sumie's initial reference image is somehow "manually selected" (e.g., "that occasion must always be

associated somehow with a previously, manually selected reference image" at response page 10, first sentence – emphasis in original). However, Sumie does NOT call for or otherwise specify any manual selection whatsoever. Sumie is silent about how the reference image is selected. The only criteria specified by Sumie is that "there is no defect" at column 7, line 56.

The Gallarda Reference

Gallarda teaches a method of selecting a defect free reference image by "arbitration", whereby two die images are compared for determining whether both are defect free, and if a defect is detected, for determining which one has the defect ("an arbitrator image is used when comparing images of two regions on a wafer to remove ambiguity as to which of the two is defective" at column 6, line 20; "a reference image can be an image of another die or cell or block, either on the same wafer ..." and of "unknown quality" at column 16, lines 12 and 14; "the reference image may be of a die with a lower probability of defects than the test image, e.g., a die near the center of a wafer is used as a reference image because it ha a lower probability of defects than a die near the edge of a wafer" at column 17, line 64; "arbitration may be combined with the defect detection process" whereby "once a defect is detected by comparison between a reference image and a test image, arbitration is performed by comparison with a third image ... to determine whether the reference image or the test image has the defect" at column 18, lines 3-10). Gallarda is able to determine whether one of two images has a defect, and which one, without using a manually selected reference image.

<u>The Gallarda and Sumie Combination</u>

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Sumie, in order to fulfill Sumie's requirements of:

a defect free "reference image";

where the reference image data is "data of an image obtained by picking up an image of a portion of the surface of the semiconductor wafer where there is no defect" at column 7, line 55;

and where an "image of the semiconductor wafer 1 in a position where no defect exists is further picked up to use as a reference image" at column 9, line 1;

by incorporating the "arbitration" method of Gallarda to initially determine a defect free image to use as the reference. That is, according to the teaching of Gallarda, it would have been obvious to modify Sumie by initially selecting and comparing (using the existing comparison capabilities of Sumie) two images to determine if one has a defect. If not, then either could be used as the reference image as both are defect fee (i.e., as taught by Gallarda). However, if one has a defect, a third image could be used to arbitrate ("arbitration is performed by comparison with a third image ... to determine whether the reference image or the test image has the defect" at Gallarda column 18, lines 3-10) where the image determined to be defect free could be used as the reference image. The teaching of Gallarda provides a way to fulfill Sumie's requirement for a defect free reference image picked up from a portion of the surface of the semiconductor wafer where there is no defect. One would be motivated to utilize the teaching of Gallarda:

1. to fulfill Sumie's requirement for a defect free reference image taken from the same semiconductor that is to be inspected;

2. to provide a fully automatic method of initially determining the defect image whereby without adding requiring any significant additional hardware to the Sumie system;

3. and to provide, in a simple and straight-forward manner, a way of accurately and quickly determining a defect free image to use as the reference using the same comparison techniques already built-in to Sumie's system.

5. Claims 90-92 and 98 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Sumie et a. (US 5,943,437 A) and Gallarda et al. (US 6,539,106 B1), and further in combination with Schemmel et al. (US 5,943,55a A).

The Sumie and Gallarda combination discloses selecting a reference die as described above. While the Sumie and Gallarda combination selects a defect free die as a reference die based on the comparison of at least first and second die images as already described, <u>Sumie does not teach storing and then combining the acceptable first and second die images to form the reference die image</u>.

Schemmel discloses system in the same field of die inspection ("detection of defects in individual silicon chips" at column 1, line 8), and same problem solving area of forming a reference die ("... create a statistical die model or "standardized" silicon chip matrix" at column 5, line 40; "statistical die model" at column 8, line 33), comprising combining first and second die images to form the reference die image ("a statistical die model matrix is obtained" and "mean gray scale values for each neighborhood of pixels" at column 8, lines 33-38; at least two

[i.e., first and second] dies images are statistically combined to form a die model, which is subsequently compared with the remaining chips on the wafer under test; also refer to column 5, lines 35-55 and column 6, lines 14-45).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the manner in which the Sumie and Gallarda combination forms his reference die image by forming a statistical die model of a plurality of dies as taught by Schemmel. That is, the Sumie and Gallarda combination (as described above) finds a defect free die to use as a reference by comparing at least first and second dies on a same wafer. When both dies images agree with one another, both are deemed acceptable (i.e., defect free) and one is used as the reference. This ensures that only defect free images are used as a reference. While this is beneficial, as modified by the teaching of Schemmel, it would have been obvious to combine those die images found to be defect free by Sumie to form a statistical die model in the manner taught by Schemmel. One would be motivated to form a statistical die model as taught by Schemmel to solve "the problem caused by the inherent defects of CCD cameras" (Schemmel, column 6, line 35), to "increase the resolution of the scan" and factor "in the differences in the background contrast of the silicon wafers" (Schemmel, column 6, lines 58-63), as well as accounting for and being robust against "different batches of silicon wafers" (Schemmel, column 10, line 55), in addition to many other motivating factors described throughout the Schemmel references.

6. Claims 76, 82, 83, 86, 87 and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Sumie et al. (US 5,943,437 A) and Gallarda et al. (US 6,539,106 B1), and further in combination with Miyazaki (US 6,031,607 A).

The Sumie and Gallarda combination discloses subtracting first and second die images ("difference is calculated pixel by pixel" at column 5, line 31) as applied to claims 73, 81 and 90 above.

Regarding claims 82, 86 and 93, Sumie does not disclose <u>creating a histogram from the image brightness data</u>.

Regarding claim 76, 83, 87 and 93, Sumie does not disclose the difference image analysis comprising a slope detector determining whether the slope of a histogram changes <u>from negative to positive.</u>

Miyazaki teaches all of these elements. Miyazaki discloses a semiconductor wafer inspection system ("defect inspection system" at column 1, line 7) comprising defect detection circuitry that analyzes a difference image ("difference image is formed" at column 14, line 64) by generating histogram data from the difference image ("difference image providing the brightness histogram" at column 15, line 6; figures 17 and 18) and analyzing the slope of the histogram data to identify a region over which the slope of the histogram changes (first, the initial slope on the dark end of the histogram is analyzed; i.e., "the amount of the slope of this line is calculated to obtain the absolute value" at column 15, line 4; then, a threshold is set in dependence on this slope as described at column 15, line 42-50, and a "portion brighter than a given uniform brightness (threshold value) is recognized as a defect" at column 15, line 34; in the context of this quote, and looking at figure 17 for example, the brightness peaks that appear

in the histogram at areas that are greater than threshold "P1" are regarded as defects, or potential defects; if there were no peaks greater than P1, and thus no slope changes after the initial slope, then the difference image would be considered defect free; the peaks appearing in figure 17 that are greater than P1 are changes in the histogram slope, and represent potential defects, thus meeting the claim requirements).

It would have bee obvious at the time the invention was made to one of ordinary skill in the art to analyze the difference image of the Sumie and Gallarda combination, using the histogram techniques as taught by Miyazaki, in order to determine whether a defect exists in one of the dies, and thereby gain the benefit of the Miyazaki analysis which "permits the individual setting of threshold value for portion of much noise and portion of less noise, producing the pattern defect inspection with high accuracy and enlarging the object of inspection" (Miyazaki, column 15, line 55).

7. Claim 98 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sumie et al. (US 5,943,437) and Gallarda et al. (US 6,539,106 B1), and further in combination with Khalaj et al. (US 5,513,275).

The Sumie and Gallarda combination discloses subtracting first and second die images ("difference is calculated pixel by pixel" at column 5, line 31).

While Sumie requires the formation of a reference image ("the reference image … to be stored" at column 7, line 50), Sumie does not describe combining two or more die images to form a reference image.

Khalaj discloses a die inspection system (column 2, lines 45-55) comprising combining two or more die images to form a reference image by "averaging among all of the blocks in image" at column 6, line 53, where "the amount of noise and the effect of the defects are reduced considerably" at line 54.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify the Sumie and Gallarda combination according to the Khalaj teaching, by averaging multiple defect free dies in order to form the "reference image" required by Sumie, thereby reducing the effect of noise, and smoothing out the effect of defects in the dies, thereby providing a more accurate, defect free reference image.

8. Claims 78, 96 and 97 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sumie et al. (US 5,943,437) and Gallarda et al. (US 6,539,106 B1), and further in combination with Berezin et al. (US 5,539,752).

The Sumie and Gallarda combination discloses subtracting first and second die images ("difference is calculated pixel by pixel" at column 5, line 31).

While Sumie requires an analysis of the difference image ("agree within a specified tolerance" at column 8, line 56), Sumie does not teach the calculation of defect density.

Many types of "tolerances" are well known in the art of manufacturing inspection, and specifically wafer inspection, including tolerances for defect density. Berezin discloses semiconductor wafer inspection (figure 1) wherein Berezin teaches providing a warning when "defect density, or number of defects per die, exceeds preselected parameters" at column 3, line 52, such as "when the number of defects of a certain defect type for a given die exceed a

threshold value, or when the defect density for a certain defect type exceeds a threshold value, thereby indicating yield-detracting operations of the manufacturing process" at column 5, lines 5-13.

It would have been obvious a the time the invention was made to one of ordinary skill in the art to include a tolerance for "defect density", as one of the "specified tolerances" required by Sumie in the Sumie and Gallarda combination, in order to flag potential defects between dies, and to flag yield-detracting operations of the manufacturing process so that the operator can take corrective action.

9. Claims 76, 82-89 and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sumie et al. (US 5,943,437) and Gallarda et al. (US 6,539,106 B1), and further in combination with Brecher et al. (US 5,544,256).

The Sumie and Gallarda combination discloses subtracting first and second die images ("difference is calculated pixel by pixel" at column 5, line 31).

While Sumie requires an analysis of the difference image ("agree within a specified tolerance" at column 8, line 56), Sumie does not teach determining unacceptable data by forming a histogram of the difference image, and determining a negative to positive slope change.

Brecher discloses a system for wafer defect detection and classification (figure 1) comprising determining unacceptable data by forming a histogram (figure 15) of a difference image ("distribution of pixel in the difference image [original image minus golden template]" at column 13, lines 25-30), and determining a negative to positive slope change (Brecher determines the values $\Delta_{positive}$ and $\Delta_{negative}$, which are the average values of the positive and

negative difference distributions as seen at figure 15 and described at column 13, lines 35-45. The "average" values exist right at the center of the distributions where the slopes changes from negative to positive. Brecher uses these values to determine an "interior contrast magnitude" at column 13, line 38, which is a "measurement for a defect in a patterned semiconductor wafer" at column 14, line 11, as listed in Table 5, at column 15. In addition, Brecher uses this technique to decide whether a "defect is dark or light" (column 13, line 5) in order to classify the defect (column 4, lines 35-50), as defect classification has become an "essential part" of the manufacturing process "where defect detection is critical", as "classification provides the information necessary to correction process or production problems" (column 1, lines 15-25; also refer to columns 14-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize the histogram technique taught by Brecher, in order to both determine the existence of a defect in the difference image of the Sumie and Gallarda combination, and to classify the defect thereby providing information necessary to correct production problems. Regarding claims 84, 85, 88 and 89, Brecher further determines defect size and density (see Tables 1 and 3) and it would have been obvious to utilize these parameters in the determination and classification of defects in the Sumie defect image for the same reasons and motivation.

10. Claims 77, 94 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Sumie et a. (US 5,943,437 A) and Gallarda et al. (US 6,539,106 B1), and further in combination with Michael (US 5,640,200 A).

The Sumie and Gallarda combination does not teach a size detector for determining whether a size of an anomalous region exceeds a predetermined allowable size.

Michael discloses a system in the same field of optical inspection (figure 7) and same problem solving area of determining defects in a difference image (see "difference image" at column 10, line 21) comprising the determination of a defect size within the difference image ("defect size" at column 15, line 60; "measuring ... area" at column 16, line 30; see equations 10a and 10b at line 45). Michael states that use of geometric criteria, such as size and area, impose "additional criteria to prevent false alarms" (column 15, line 58).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to impose size as a defect criteria as taught by Michael, for the determination of potential defects on a die as identified by the difference image of Sumie, in order to impose additional criteria for determining a defect to prevent false alarms, and the false determination of a defect in an otherwise good wafer die.

11. Claims 94 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Sumie et a. (US 5,943,437 A), Gallarda et al. (US 6,539,106 B1) and Schemmel et al. (US 5,943,551 A) as applied to claim 90 above, and further in combination with Michael (US 5,640,200 A).

Sumie and Gallarda as modified by Schemmel does not teach a size detector for determining whether a size of an anomalous region exceeds a predetermined allowable size.

Michael discloses a system in the same field of optical inspection (figure 7) and same problem solving area of determining defects in a difference image (see "difference image" at

column 10, line 21) comprising the determination of a defect size within the difference image ("defect size" at column 15, line 60; "measuring ... area" at column 16, line 30; see equations 10a and 10b at line 45). Michael states that use of geometric criteria, such as size and area, impose "additional criteria to prevent false alarms" (column 15, line 58).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to impose size as a defect criteria as taught by Michael, for the determination of potential defects on a die as identified by the difference image of Sumie, Gallarda and Schemmel, in order to impose additional criteria for determining a defect to prevent false alarms, and the false determination of a defect in an otherwise good wafer die.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (US 2004/0057611 A1), while not prior art, is pertinent as teaching the selection of a reference die by image subtraction.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Werner whose telephone number is 703-306-3037. The examiner can normally be reached on M-F, 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo H. Boudreau can be reached on 703-305-4706. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Werner
Primary Examiner
Art Unit 2621
February 1, 2005

BRIAN WERNER
PRIMARY EXAMINER